Simulation of Signal Conditioner Circuit for Water Quality Monitoring Device using Current Differential Trans conductance Amplifier

Armaan singh

[1]Assitant Professor
[1] Mizoram, India
[1] armaansingh@gmail.com*
* corresponding author

ARTICLE INFO

Article History:
Received Jan 1, 2019
Revised June 15, 2019
Accepted Oct 12, 2020

Keywords:
Chemical Oxygen Demand, Low Pass filter, CMOS, CDTA, Xilinx

Correspondence:
E-mail: armaansingh@gmail.com

ABSTRACT

A new configuration realizing water quality monitoring device using photo catalytic sensor for the determination of chemical oxygen demand (COD)involving CMOS current differencing trans conductance amplifier (CDTA) based low pass filter free from trans conductance variation is proposed. The circuit uses four CDTA's as active elements and together with two capacitors and one resistors as passive elements. The use of this active component makes the implementation simple and attractive. The functionality of the circuit is tested using Tanner simulator version 15 for a 70nm CMOS process model also the transfer function realization is done on MATLAB, the Very high speed integrated circuit Hardware description language(VHDL) code for the same scheme is simulated on Xilinx ISE and various simulation results are obtained. Simulation results are included to demonstrate the results.

1. INTRODUCTION

Monitoring the pH of water resources and sewage system for water pollution is typical and necessary task in today's overdeveloped scenario. Now a day's we have Semiconductor based micro sensors which are easily available and economical and able to react with the ion concentration, in other words activity of the ions. A photo catalytic sensor for the determination of chemical oxygen demand (COD) with flow injection analysis (FIA) based on the photo catalysis of organic compounds in the presence of titanium dioxide (TiO2) beads in a photochemical column is used to measure the quantity of COD. The sensor was developed in conjunction with TiO2 beads in the photochemical column and with an oxygen electrode as the sensing part. The sensor signal was observed as a result of the detection of dissolved oxygen changes due to photo catalytic oxidation of organic compounds in the sample solution. This sensor responded linearly to the CODMn of artificially treated wastewater (AWW) in the range of 0.12–8 ppm [1-3]. Photo catalytic sensor has been found several drawbacks related to thermal dependency, long-term drift, linearity, dynamic range. To improve the accuracy in the biomedical applications, it is necessary to find the compensation method to make the applications free from these effects. In order to capture the output response of the photo catalytic sensor, a readout interface is necessary. In this paper a new readout interface circuit having greater linearity, low power consumption, large bandwidth, by using current mode circuits (CMC's) is proposed.

Conventional water quality monitoring applications are made up of voltage mode circuits (VMC) based on op-amps and OTA's [3-5]. These applications are suffer from low band widths (BW's) arising due to stray and circuit capacitances. Also the need for low voltage, low power circuits makes these circuits not suitable for water quality monitoring as these circuits required the minimum bias voltage depends on the threshold voltage of the MOSFETs. However, with the advancement in the analog VLSI new analog devices are based on currents are developed called current mode circuits (CMC's). These circuits have a significant advantage of low power, low voltages and can operate over wide dynamic range. These circuits, CMC can offer to the designer large bandwidths, greater linearity, wider dynamic range, simple circuitry and low power consumption. Current feedback op-amps (CFOAs), operational floating conveyors (OFCs) and current conveyors (CCs) etc. are popular CMC configuration and most widely used structure among them is CDTA, extension of the second-generation current conveyor (CCII). Hence, we decided to use the CDTA in the proposed scheme.

2. SEMICONDUCTOR PHOTO CATALYSIS

Explaining the aim of semiconductor photo catalysis is to effectively detoxify toxious organic pollutants. UV or visible light is used to create electron/hole pairs in semiconductor. The electron then react with oxygen in the sample to form O2- and hole reacts with surface hydroxyl groups to form OH. radicals. The radical species then attack the organic molecule which is eventually oxidized to CO2 and H2O. It will produce HCL if the organic molecule contains chlorine.

Photo catalysis is an efficient method for the degradation and mineralization of organic compounds [6-8]. It has been the subject of numerous studies to obtain a better understanding of the mechanisms of the reactions involved [10]. A semiconductor particle is believed to have a filled valence band separated from a vacant conduction band by a gap whose energy is Eg. When irradiated with a light source, whose energy exceeds Eg, an electron is promoted from the valence to the conduction band, leaving behind a positive hole. Upon migration to the surface, the electron would reduce any available species. In contrast, when the hole reaches the surface, it would react with water to produce hydroxyl radicals. These radicals play an important role in oxidizing organic pollutants. Molecular oxygen dissolved is also an essential component because it acts as scavenger of the photo generated electrons, forming a superoxide radical ion, and further reacting with transient radicals leading toward CO2 formation [11-14]. It was found that photo catalytic activity is almost completely suppressed in the absence of oxygen and the concentration of oxygen has a profound effect on the rate of photo catalyzed decomposition of organic compounds. Many of photo catalytic processes apply the TiO2 as a photo catalyst because it is non-photo corrosive, non-toxic, and capable of the photo oxidative destruction of most organic pollutants [15-17]. It is well known that the TiO2 photo catalysis leads to stoichiometric photo mineralization of organic compounds

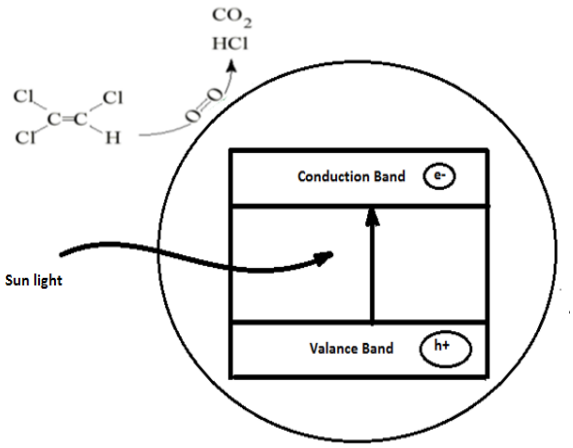

Fig.1: Diagram to show Photocatalysis

3. CDTA

In Since an introduction of the current differencing trans conductance amplifier (CDTA) in 2003, it has been acknowledged to be a versatile current-mode active building block in designing analog circuits [18]. This device that has two current inputs and two kinds of current output provides an easy implementation of current-mode active filters [19]. It also exhibits the ability of electronic tuning by the help of its trans conductance gain (gm). All these advantages together with its current-mode operation nature make the CDTA a promising choice for realizing the current-mode filters. As a result, a variety of CDTA applications has also been considered by various researchers [20-23].

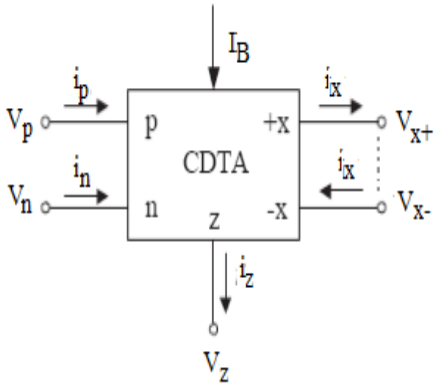

Fig. 2 : Electrical symbol of CDTA

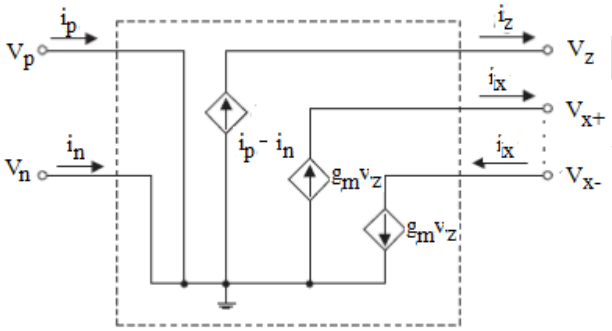

Figure.2(b)Equivalent circuit

Its input-output terminal relations are given by the following matrix equation:

$$\begin{pmatrix} I_z \\ V_w \\ I_x \\ V_{p(n)} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & (-)1 \\ 1 & 0 & 0 & 0 \\ g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_z \\ I_w \\ V_x \\ I_{p(n)} \end{pmatrix}$$

4. CMOS realization of CDTA

The circuit representation and the equivalent circuit of the CDTA are shown in Fig.2. The terminal relation of the CDTA can be characterized by the following set of equations (1-3).

Vp = Vn = 0 (1)

iz = ip - in (2)

and ix = gm Vz = gm Zz iz. (3)

where p and n are input terminals, z and ±x are output terminals, gm is the trans conductance gain, and Zz is an external impedance connected at the terminal z.

According to above equation and an equivalent circuit of Fig.2(b), the current flowing out of the terminal z (iz) is a difference between the currents through the terminals p and n (ip-in). The voltage drop at the terminal z is transferred to a current at the terminal x (ix) by a trans conductance gain (gm), which is electronically controllable by an external bias current (IO). These currents, which are copied to a general number of output current terminals x, are equal in magnitude but flow in opposite directions. Although there are several techniques to realize the CDTA, one possible bipolar realization is shown in Fig.3 [24-25]. It mainly comprises a current differencing circuit formed by two current followers Q1-Q9, a basic current mirror Q10-Q11, and a multiple-output trans conductance amplifier Q12-Q42. In this case, the trans conductance gain gm of the CDTA is directly proportional to the external bias current IO, which

can be written by

$$g_m = \frac{I_B}{2V_T} \quad (4)$$

where V_T = 26 mV at 27oC is the thermal voltage.

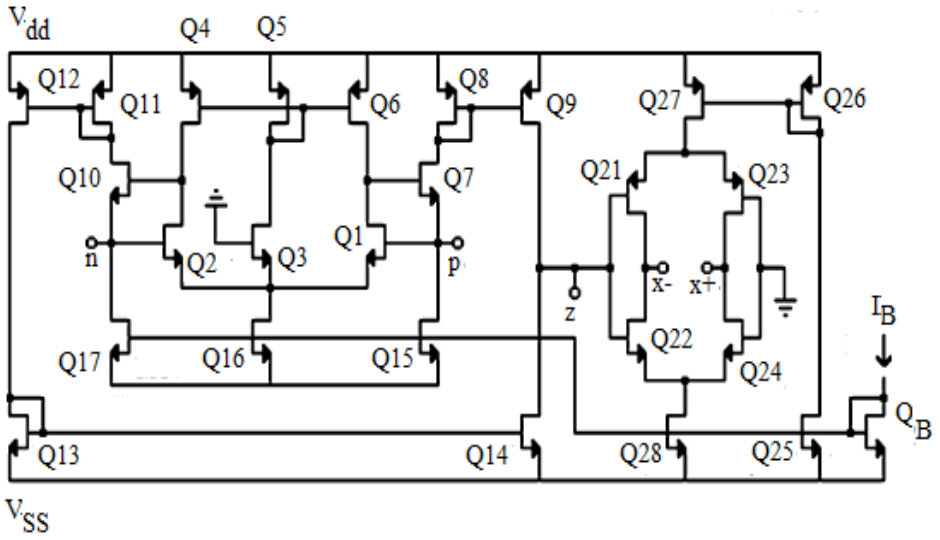

Fig. 3: Circuit diagram of CMOS based CDTA

Process parameter of CDTA used are given in the table 1

Table 1:- Process parameter

Parameters	CDTA
CMOS technology(nm)	70
Power supply(VDD, GND)	5V-0V
No. of Mosfets	32
Average power dissipation	5.337467e-001 watts
Max power	5.352302e-001
Min power	5.315526e-001
X terminal input resistance	9 ohm

5. Device Description and Mathematical Modeling

The Block diagram of the proposed scheme is given below it consists of (1) Photo Catalytic Sensor (2) CDTA based Low Pass filter (3)Current follower (4)Current mirror circuit for the proper biasing of current conveyors (4)LCD display to show the output thus obtained.

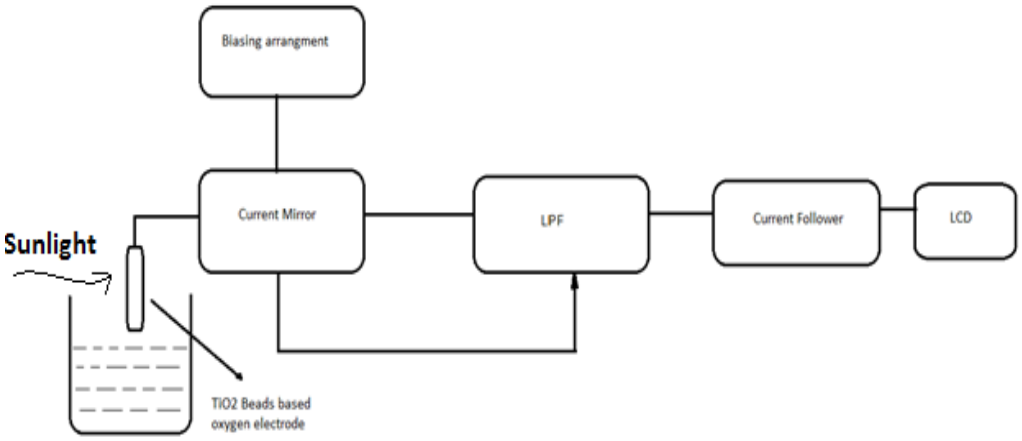

Fig. 4 Block diagram of proposed scheme

The block diagram of the proposed scheme is shown below it consists of one CDTA, two capacitors, one resistors, photo catalytic sensor , Current Mirror One of the drawbacks of the Current conveyor device is that its trans conductance (g_m) varies often with the I_{bias}. To make the device free from trans conductance variation we used current mirrors along with the current conveyors which are capable of providing the constant I_{bias} and thereby, making the device free from change of trans conductance effect. Various kinds of Current mirrors are found but, to make the design low power PMOS bulk-driven cascade current mirror is used. The topology of the low-voltage PMOS bulk-driven cascade current mirror is used to control the gm of the CDTA.

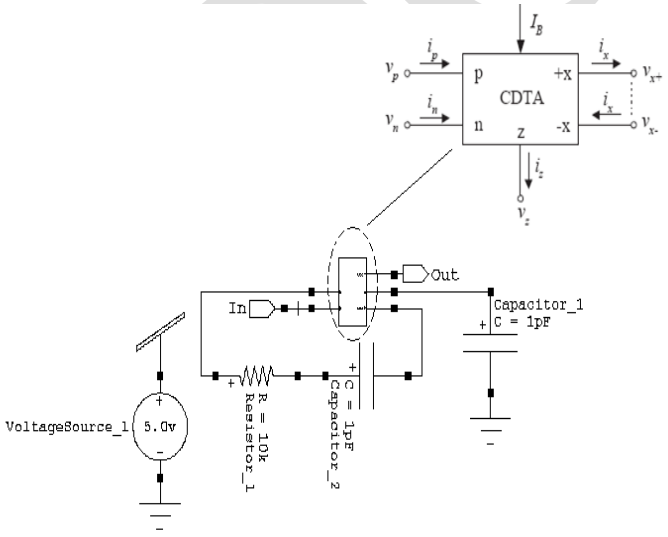

Fig.5 Circuit diagram of LPF using three CDTA's and passive components

The transfer function of the proposed scheme is calculated as below

$$I_o = \frac{b_0 I_1 - (b0 + aS) I_2}{D(S)} \qquad (5)$$

$$D(S) = S^2 + b_1 S + b_0 \qquad (6)$$

Where b0 = $\frac{g_m}{RC_1C_2}$, b1= $\frac{1}{RC_1}$, a= $\frac{g_m}{C_2}$

From (6) ω_O and Q of the proposed circuit is given as

$$\omega_O = \sqrt{\frac{g_m}{RC_1C_2}} \quad \text{(Natural frequncy)}$$

$$Q = \sqrt{\frac{g_m RC_1}{C_2}} \quad \text{(Quality factor)}$$

$B=\frac{W_o}{Q}$ (Bandwidth)

Take the typical values of Passive elements R =R1=R2 =1kΩ, C1= C2=20pF g_m=800µs we get,

For optimization take

In=$\frac{I_1}{2}$ and I2=0

$I_{LP} = \frac{2b_o}{D(S)}$

bo = $\frac{g_m}{RC_1C_2} = 2\times 10^{15}$

$$I_{LP} = \frac{2b_o}{D(S)} = \frac{2 \times 10^{15}}{S^2 + 5 \times 10^7 S + 2 \times 10^{15}}$$

The nyquist and Bode plot of the above transfer function is plotted with the help of MATLAB .

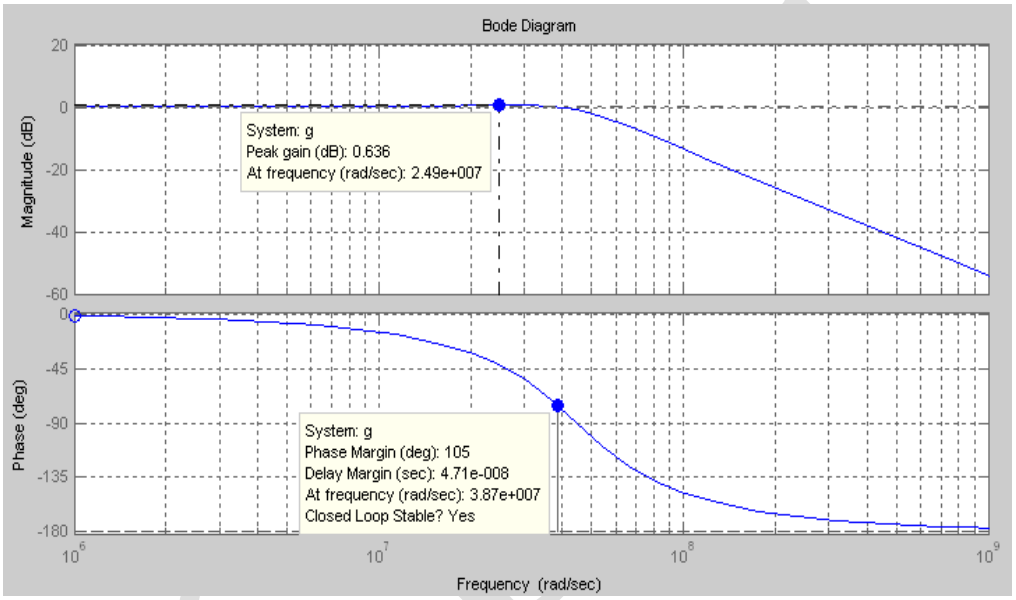

Fig.6 bode plot of the above transfer function

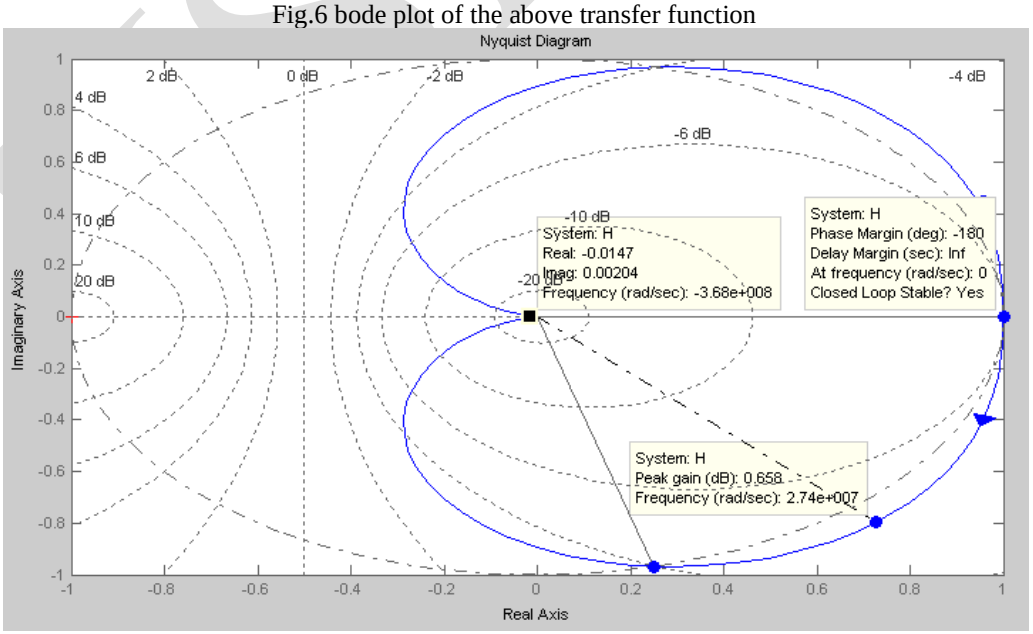

Fig.7 nyquist plot of the above transfer function

Figure 6-7shown above justify that the transfer function of the system is closed loop stable with phase margin of 68.5 degree at frequency 3.5 MHz.

6. Current Mirror

One of the drawbacks of the Current conveyor device is that its trans conductance (gm) varies often with the Ibias . To make the device free from trans conductance variation we used current mirrors along with the current conveyors which are capable of providing the constant Ibias and thereby, making the device free from change of trans conductance effect. To make the design low power PMOS bulk-driven cascade current mirror (PMOS BDCCM) is used. The topology of the low-voltage PMOS bulk-driven cascade current mirror is shown in Figure.8.

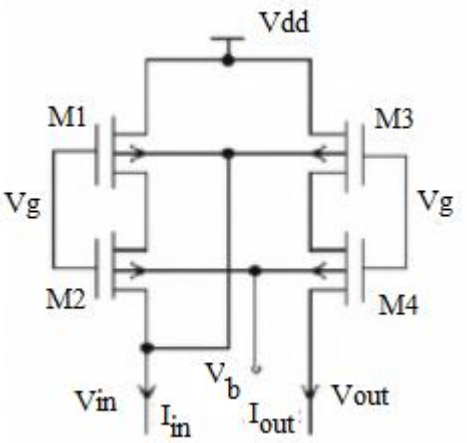

Fig.8 PMOS bulk-driven cascade current mirror

Since the source drain voltage of M4 is unrestricted M4 may work in linear or saturation region obviously minimum output voltage drop BDCCM is lower than GDCCM. The bulk-driven technique may eliminate the limitation of the threshold voltage on the signal channel effectively, thereby reducing the supply voltage required by CMOS analog IC. Compared with the normal gate-driven CMs, the low-voltage BDCCM reduces the input/output voltage drop greatly and has a good input/output resistance characteristic along with a better current driving ability.

7. SIMULATION AND RESULTS ANALYSIS

Simulation of a readout interface circuit for water quality monitoring device using photo catalytic sensor involving second generation current conveyors have been carried out on Tanner simulator version 15 for a 70nm CMOS process model . In the proposed circuit, following typical values for passive components were chosen Figure 9: R 9 =1kΩ, C1= C2=20pF g_m=800µs. The proposed readout circuit is modeled using Tanner Tool Version 15 in 70 nm technology and shown in Figure 8.The output response of the device with respect to the time i.e transient analysis shown in Figure 9 justify the device is highly linear. The power results obtained when the device is simulated 70nm technology is shown in the appendix at the end of the paper and it is found that the device consumes the average power of 4.531175e-002 watts. The device is found stable as shown in the mathematical modeling by the analysis of the transfer function and by bode and nyquist plot.

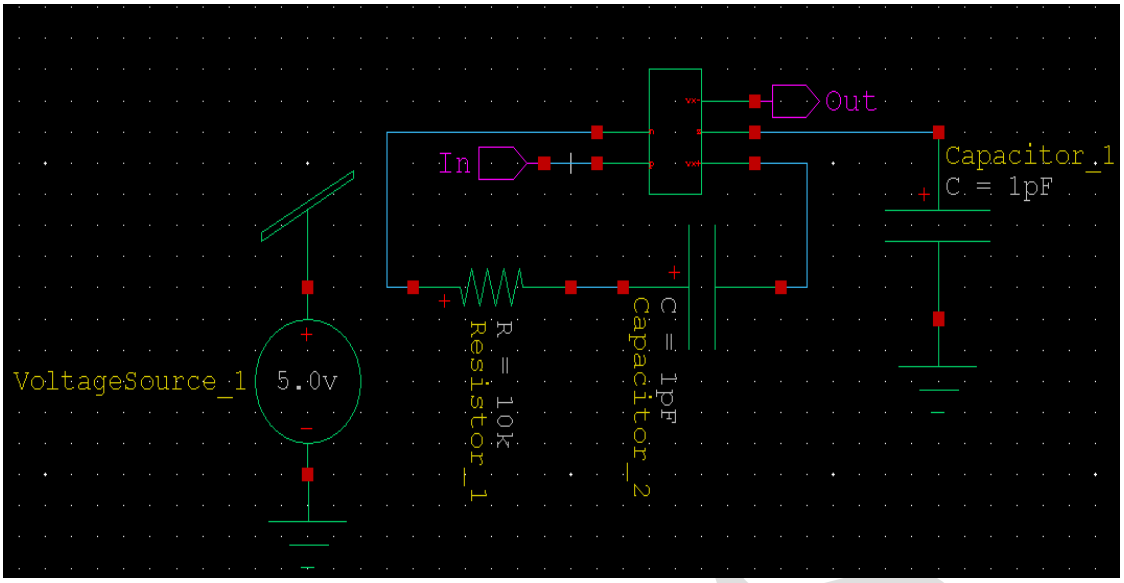

Fig.9 Circuit diagram of proposed scheme

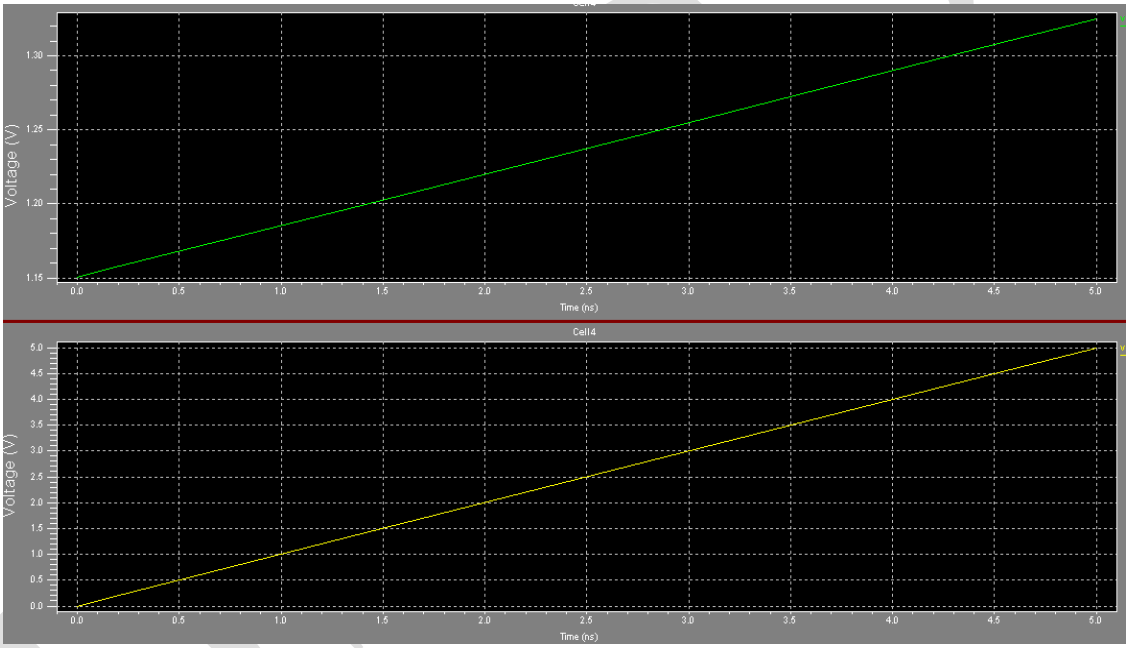

Fig.10 Transient analysis

8. Conclusion

In this paper, a new interface readout circuit employing CMOS current differencing trans conductance amplifier (CDTA) is proposed. The second-generation current conveyor introduced is a convenient building block that provides a simplified approach to the design of linear analog systems. The bulk-driven technique used to control the trans conductance effect of CDTA may eliminate the limitation of the threshold voltage, thereby reducing the supply voltage required by CMOS analog IC. Results of computer simulations and the comparison with experimental data and with transistor-level simulation demonstrated an accuracy of the approach. All the results are in good agreement with the theoretical analysis. This study may be extended and more improvement in terms of power and size can be achieved at layout level and thus more effective results may be obtained.

REFERENCES

[1] P. Whig and S. N. Ahmad (2014), Simulation of linear dynamic macro model of photo catalytic sensor in SPICE, Compel the Int. J. Comput. Math. Electric. Electron. Eng. 33, 611–629.
[2] P. Whig and S. N. Ahmad(2014), Development of Economical ASIC For PCS For Water Quality Monitoring , JCSC Vol. 23, No. 6, pp.1-6.
[3] G W Roberts, A S Sedra(1989), All current-mode frequency selective circuits., Electronics Letters, 1989, 25(12),pp:759-761.
[4] A Sedra, K. A Smith (1970). second-generation conveyor and its applications,IEEE Transconductions on Circuit Theory. 1970, CT-17,pp: 132-134.
[5] C.A.Karybakas, C.A.Papazoglou(1999). Low-Senstive CCII-Based Biqua-dratic Filters Offering Electronic Frequency Shifting. IEEE Transactions on Circuits And Systems-II: Analog And Digital Signal Processing, 1999, 46(5),pp: 527-539.
[6] A Khan, S Bimal, K K Dey(2005). Novel RC sinusoidal using second generation current conveyor. IEEE Transactionson Instrumentation and Measurement, 2005, 54(6),pp:2402-2406.
[7] P. Whig and S. N. Ahmad(2012), "Performance analysis of various readout circuits for monitoring quality of water using analog integrated circuits," International Journal of Intelligent Systems and Applications, vol. 11, pp. 91–98.
[8] W Chiu, S I Liu, H W Tsao, J J Chen(1996). CMOS differential difference current conveyors and their applications. IEEE Proceedings G: Circuits Devices Systems, 1996, 43(2),pp:91-96
[9] H O Elwan, A M Soliman(1997). Novel CMOS differential voltage current conveyor and its applications. IEEE Proceedings G: Circuits Devices Systems, 1997, 144(3),pp: 195-200
[10] EI-Adawy A A, Soliman A M, Elwan H O(2000). A novel fully differential current conveyor and applications for analog VLSI. IEEE Transaction on circuits and systems-II:Analog and digital signal processing, 2000, 47(4),pp: 306~313.
[11] Cecilia Jimenez-Jorquera, Jahir Orozoo, Antoni Baldi (2010), ISFET based Microsensors for Environmental Monitoring, Journal of Sensors ISSN 1424-8220, pp: 61-83.
[12] F.M.Klaassen and W. Hes (1986), On the Temperature Coefficient of the MOSFET Threshold Voltages, Solid-State Electronics, pp: 787-789.
[13] P. Whig and S N. Ahmad(2012) , "DVCC based Readout Circuitry for Water Quality Monitoring System," International Journal of Computer Applications (IJCA), vol. 49, no. 22, pp. 1-7.
[14] P.Bergveld (1970), Development of an Ion-sensitive Solid-state Device for Neurophysiologic Measurements, IEEE Trans. Biomed. Eng.pp: 70-71.
[15] D.MWilson,S.Hoyt,J.Janata,K.Booksh,and L.obando,(2001)"Chemical sensors for portable ,handheld field instruments,'IEEE Sensors j.,vol.1,no.4,pp256-274.
[16] P.Bergveld,(2000) "Thirty years of ISFETOLOGY what happened in the past 30 years and what may happen in the next 30 years,'Sens.Actuators B, Vol . 88,pp1-20.
[17] S.jamasb,S.D. Collins , and R.L Smith(1998) ,"A physical model for threshold voltage insability in SI3N4 gate H+ sensitive FETs,"IEEE Tran. Electron Devices, Vol. 45 no. 6 ,pp.1239-1245.
[18] P. Whig and S. N. Ahmad (2011),"On the Performance of ISFET-based Device for Water Quality Monitoring,". International Journal of Communications, Network and System Sciences ISSN 1913-3715, vol. 4, pp: 709 -719.
[19] L.J Bousse,D.Hafeman, and N.Tran(1991),'Time Dependence of the chemical response of silicon nitride surfaces ,"Sens. Actuators B,Vol.1,pp.361-367.
[20] P.R.Barabash,R.S.C Cobbold and W.B.wlodarski(1987),'Analysis of the threshold voltage and its temperature dependence in electrolyte-in sulator –semiconductor field effect transistor,"IEEE trans.Electron Devices ,vol.34 ,no.6 pp 1271-1282.
[21] Haron, Nazleeni Samiha; Mahamad, Mohd Khuzaimi B.; Aziz, Izzatdin Abdul; Mehat, Mazlina; (2008), " A system architecture for water quality monitoring system using wired sensors." Vol: 4, pp: 1–7.
[22] Sergio Martinoia and Giuseppe Massobrio (2002), A Behaviour Macro-Model of the ISFET in SPICE, Sensors and Actuators B, pp: 182-189.
[23] B. Palan, F.V.Santos, and J.M.Karam (1999), New ISFET Sensor Interface Circuit for Biomedical Applications, Sensors and Actuators B, pp: 63-68.
[24] C.H.Yang, W.Y.Chung, K.K.Lin, D.G.Pijanowska and W. Torbicz (2003), A Low-Power Telemetric System Design for ISFET-Based Sensor Array Applications, European Conf. on Circuit Theory and Design. pp: 260-263.
[25] S. Jamasb, "An analytical technique for counteracting drift in ion-selectivefield effect transistors (ISFETs),2004" IEEE Sensors J., vol. 4, no. 6,pp. 795–801.

Appendix

Simulation results

```
=========================================
*                Synthesis Options Summary                *
=========================================
---- Source Parameters
Input File Name                    : "Cell1.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "Cell1"
Output Format                      : NGC
Target Device                      : xc3s100e-5-vq100

---- Source Options
Top Module Name                    : Cell1
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : YES
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : YES
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 24
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Library Search Order               : Cell1.lso
Keep Hierarchy                     : NO
Netlist Hierarchy                  : as_optimized
RTL Output                         : Yes
Global Optimization                : All Clock Nets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
```

```
Case Specifier                          : maintain
Slice Utilization Ratio                 : 100
BRAM Utilization Ratio                  : 100
Verilog 2001                            : YES
Auto BRAM Packing                       : NO
Slice Utilization Ratio Delta           : 5

=========================================


Power result

*  Device and node counts:
*          MOSFETs - 20          MOSFET geometries - 4
*            BJTs - 0                JFETs - 0
*          MESFETs - 0               Diodes - 0
*        Capacitors - 0            Resistors - 0
*         Inductors - 0          Mutual inductors - 0
*  Transmission lines - 0    Coupled transmission lines - 0
*     Voltage sources - 5        Current sources - 2
*            VCVS - 0                VCCS - 0
*            CCVS - 0                CCCS - 0
*    V-control switch - 0        I-control switch - 0
*      Macro devices - 0     External C model instances - 0
*        HDL devices - 0
*        Subcircuits - 0       Subcircuit instances - 0
*   Independent nodes - 12          Boundary nodes - 6
*        Total nodes - 18


*SEDIT: Analysis types DCOP 0 ACMODEL 0 AC 0 TRANSIENT 1 TRANSFER 0 NOISE 0

*WEDIT: .tran   2e-009   5e-009
TRANSIENT ANALYSIS
Time<s>                 v(in)<V>        v(out)<V>
 0.000000e+000          0.0000e+000     1.1508e+000
 1.250000e-010          1.2500e-001     1.1550e+000
 1.375000e-009          1.3750e+000     1.1983e+000
 2.926462e-009          2.9265e+000     1.2525e+000
 4.578586e-009          4.5786e+000     1.3102e+000
 5.000000e-009          5.0000e+000     1.3253e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
vdd from time 0 to 5e-007
Average power consumed -> 4.531175e-002 watts
Max power 6.167927e-002 at time 3.05e-007
Min power 3.455305e-002 at time 5e-009
* END NON-GRAPHICAL DATA
* Parsing                       0.01 seconds
* Setup                         0.00 seconds
* DC operating point            0.00 seconds
* Transient Analysis            0.06 seconds
* Overhead                      1.06 seconds
* ---------------------------------------
* Total                         1.14 seconds

* Simulation completed

* End of T-Spice output file
```